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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,355	09/11/2003	Mark F. Kelcourse	17988	7884

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TYCO TECHNOLOGY RESOURCES
4550 NEW LINDEN HILL ROAD, SUITE 140
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EXAMINER	
GUZMAN, APRIL S	
ART UNIT	PAPER NUMBER
2618	
MAIL DATE	DELIVERY MODE
09/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,355	KELCOURSE, MARK F.	
	Examiner	Art Unit	
	APRIL S. GUZMAN	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,7,9-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3,4,6,7,9-13,17,19 and 20* is/are allowed.

6)☒ Claim(s) *14 and 16* is/are rejected.

7)☒ Claim(s) *15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/11/03,11/04/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments, filed 06/19/2008, with respect to Claims 1, 3-4, 6-7, 9-17, and 19-20 have been fully considered and are persuasive. The rejection of claims 1, 3-4, 6-7, 9-17 and 19-20 has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made on claims 14 and 16 in view of Gerlach et al. (U.S. Patent # 6,518,855) in view of Khabbaz et al. (U.S. Patent 6,351,183).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Gerlach et al. (U.S. Patent # 6,518,855)**, and further in view of **Khabbaz et al. (U.S. Patent 6,351,183)**.

Consider **claim 14**, Gerlach et al. teach a single-die transmitter/receiver integrated switching circuit comprising:

a plurality of transmitter ports (column 3 lines 18-26);

a plurality of receiver ports (column 3 lines 18-26);

at least one antenna port (column 3 lines 18-26);

a plurality of integrated circuit switching elements controllable to connect one of the transmitter ports of one of the receiver ports to the antenna port while isolating the remaining ones of the transmitter and receiver ports from the antenna port, at least one of the plurality of transmitter ports and the plurality of receiver ports being at least three in number (column 2 lines 20-32, column 2 lines 41-54, column 3 lines 18-26 and column 3 lines 37-63).

However, Gerlach et al. fail to teach at least some of the integrated circuit switching elements arranged in cascaded fashion in order to reduce signal insertion loss.

In the related art, Khabbaz et al. teach at least some of the integrated circuit switching elements arranged in cascaded fashion in order to reduce signal insertion loss (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Khabbaz into the teachings of Gerlach for the purpose of amplifying weak received signals to place the signal within the optimum signal amplitude range wherein high gain, high linearity and low noise figure are desirable.

Consider **claim 16, as applied to claim 14,** Gerlach et al. as modified by Khabbaz et al. further teach wherein the integrated circuit switching elements are field effect transistors (Gerlach et al. - column 1 lines 51-62, and column 3 lines 337-63).

Allowable Subject Matter

Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 1, 3-4, 6-7, 9-13, 17, and 19-20 are allowed.

Consider **claim 1**, the best prior art of record during the examination of the present application, **Gerlach et al. (U.S. Patent # 6,518,855)** in view of **Khabbaz et al. (U.S. Patent 6,351,183),** fail to specifically teach, disclose or suggest a single-die integrated circuit for switching among a plurality of transmission ports and a plurality of receiver ports, comprising: a transmitter switching section having a plurality of transmission ports, the transmitter switching section operable to switch a selected one of the plurality of transmission ports to a transmission node; and a receiver switching section having a plurality of receiver ports, the receiver switching section operable to switch a selected one of the plurality of receiver ports to the transmission node, *wherein the receiver switching section includes at least two cascaded stages, a first cascaded stage controllable to switch the transmission node to a receiver node, and a second cascaded stage controllable to switch the receiver node to a selected one of the plurality of receiver ports*.

Gerlach teach semiconductor switching elements such as field effect transistors which are integrated on a circuit in the form of a Monolithic Microwave Circuit. The circuit is connected to at least two transmitting apparatuses and at least two receiving apparatuses in which case the transmitters and receivers respectively differ in that they operate on different frequency bands

(column 1 lines 41-67 and column 2 lines 20-54). Gerlach also teach a first transmitter which is used for frequency band 1, is connected to antenna 1, the receiver for frequency band 2 is connected to antenna 2. The circuit is constructed monolithically in an integrated manner. The switch 1 is formed by FETS 9 to 12. FETs 9 and 11 as well as 10 and 12, respectively, are working together to connect Tx Band 1 or TX Band 2 with terminal Tx. FETs 9 and 12 are controlled by varying the gate potential, FETs 11 and 10 are controlled by varying the potentials of the source of the drain (column 3 lines 18-62).

Khabbaz teach a switched amplifying device according to an embodiment of the present invention designed to amplify over a 1.8 GHz to 2 GHz frequency band and having two gain stages in a cascade configuration. The dual gain stage embodiment of the switched amplifying device comprises the amplifying FET (8), which in the dual gain stage embodiment is termed a first amplifying FET (8), and a second amplifying FET (108). The first amplifying FET (8) produces an amplified signal at the drain (9). The switched amplifying device further comprises a second amplifying FET having a gate (111) which is coupled to receive and further amplify the amplified signal to achieve higher gain than in the single gain stage embodiment shown in FIG. 4 of the drawings. The drain (9) of the first amplifying FET (8) is connected to the gate (111) of the second amplifying FET (108) through a matching series capacitor (50) (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).

These teachings clearly differ from the claimed invention, therefore, claim 1 is considered novel and non-obvious over the prior art and therefore is allowed.

Claims 3-4 and 6 depend upon allowable claim 1, therefore, these claims are also allowed.

Consider **claim 7**, the best prior art of record during the examination of the present application, **Gerlach et al. (U.S. Patent # 6,518,855)** in view of **Khabbaz et al. (U.S. Patent 6,351,183),** fail to specifically teach, disclose or suggest a single-die multiband switch for wireless communication, comprising: an antenna port; a plurality of transmitter ports, for each transmitter port a switching topology operable to switch the last said transmitter port to the antenna port; and a plurality of receiver ports, for each receiver port a switching topology operable to switch the last said receiver port to the antenna port; wherein at least one of the switching topologies comprises *a plurality of field effect transistors having their current paths coupled in series between an associated transmission port and the antenna port, a control signal for the at least one switching topology controlling the at least one switching topology to selectively connect or isolate a respective transmitter port from the antenna port.*

Gerlach teach semiconductor switching elements such as field effect transistors which are integrated on a circuit in the form of a Monolithic Microwave Circuit. The circuit is connected to at least two transmitting apparatuses and at least two receiving apparatuses in which case the transmitters and receivers respectively differ in that they operate on different frequency bands (column 1 lines 41-67 and column 2 lines 20-54). Gerlach also teach a first transmitter which is used for frequency band 1, is connected to antenna 1, the receiver for frequency band 2 is connected to antenna 2. The circuit is constructed monolithically in an integrated manner. The switch 1 is formed by FETS 9 to 12. FETs 9 and 11 as well as 10 and 12, respectively, are working together to connect Tx Band 1 or TX Band 2 with terminal Tx. FETs 9 and 12 are controlled by varying the gate potential, FETs 11 and 10 are controlled by varying the potentials of the source of the drain (column 3 lines 18-62).

Khabbaz teach a switched amplifying device according to an embodiment of the present invention designed to amplify over a 1.8 GHz to 2 GHz frequency band and having two gain stages in a cascade configuration. The dual gain stage embodiment of the switched amplifying device comprises the amplifying FET (8), which in the dual gain stage embodiment is termed a first amplifying FET (8), and a second amplifying FET (108). The first amplifying FET (8) produces an amplified signal at the drain (9). The switched amplifying device further comprises a second amplifying FET having a gate (111) which is coupled to receive and further amplify the amplified signal to achieve higher gain than in the single gain stage embodiment shown in FIG. 4 of the drawings. The drain (9) of the first amplifying FET (8) is connected to the gate (111) of the second amplifying FET (108) through a matching series capacitor (50) (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).

These teachings clearly differ from the claimed invention, therefore, claim 7 is considered novel and non-obvious over the prior art and therefore is allowed.

Claims 9-13 depend upon allowable claim 7, therefore, these claims are also allowed.

Consider **claim 17**, the best prior art of record during the examination of the present application, **Gerlach et al. (U.S. Patent # 6,518,855)** in view of **Khabbaz et al. (U.S. Patent 6,351,183),** fail to specifically teach, disclose or suggest a method of switching one of a plurality of transmitters and a plurality of receivers to a transmitter/receiver antenna, comprising the steps of: connecting each transmitter to a respective one of a plurality of transmitter ports formed on a single integrated circuit die; connecting each receiver to a respective one of a plurality of receiver ports formed on the die; controlling a selected one of a plurality of switching topologies each associated with a respective one of the transmitter and receiver ports to connect a respective

selected one of the transmitter and receiver ports to an antenna port formed on the die; controlling other ones of the switching topologies to isolate others of the transmitter and receiver ports from the antenna port; *arranging at least some of the switching topologies in cascaded stages including a first stage coupled to the antenna port and a last stage coupled to a plurality of the transmitter or receiver ports; connecting a selected one of the transmitter or receiver ports to the antenna port by switching on the first stage and switching on a switch associated with the selected one of the transmitter or receiver ports wherein the switch associated with the selected one of the transmitter or receiver ports is a portion of the last stage*; and switching off the remaining switching topologies and other switches in the last stage.

Gerlach teach semiconductor switching elements such as field effect transistors which are integrated on a circuit in the form of a Monolithic Microwave Circuit. The circuit is connected to at least two transmitting apparatuses and at least two receiving apparatuses in which case the transmitters and receivers respectively differ in that they operate on different frequency bands (column 1 lines 41-67 and column 2 lines 20-54). Gerlach also teach a first transmitter which is used for frequency band 1, is connected to antenna 1, the receiver for frequency band 2 is connected to antenna 2. The circuit is constructed monolithically in an integrated manner. The switch 1 is formed by FETS 9 to 12. FETs 9 and 11 as well as 10 and 12, respectively, are working together to connect Tx Band 1 or TX Band 2 with terminal Tx. FETs 9 and 12 are controlled by varying the gate potential, FETs 11 and 10 are controlled by varying the potentials of the source of the drain (column 3 lines 18-62).

Khabbaz teach a switched amplifying device according to an embodiment of the present invention designed to amplify over a 1.8 GHz to 2 GHz frequency band and having two gain

stages in a cascade configuration. The dual gain stage embodiment of the switched amplifying device comprises the amplifying FET (8), which in the dual gain stage embodiment is termed a first amplifying FET (8), and a second amplifying FET (108). The first amplifying FET (8) produces an amplified signal at the drain (9). The switched amplifying device further comprises a second amplifying FET having a gate (111) which is coupled to receive and further amplify the amplified signal to achieve higher gain than in the single gain stage embodiment shown in FIG. 4 of the drawings. The drain (9) of the first amplifying FET (8) is connected to the gate (111) of the second amplifying FET (108) through a matching series capacitor (50) (Figure 8, column 6 lines 55-67 and column 7 lines 1-40).

These teachings clearly differ from the claimed invention, therefore, claim 17 is considered novel and non-obvious over the prior art and therefore is allowed.

Claims 19-20 depend upon allowable claim 17, therefore, these claims are also allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: see PTO-892 Notice of References Cited.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

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Hand-delivered responses should be brought to

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Randolph Building

401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the examiner should be directed to April S. Guzman whose telephone number is 571-270-1101. The examiner can normally be reached on Monday - Thursday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Anderson can be reached on 571-272-4177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/April S. Guzman/
Examiner, Art Unit 2618

/Matthew D. Anderson/
Supervisory Patent Examiner, Art Unit 2618